IN THE CLAIMS

Please amend the claims as follows:

1. (original) A method of manufacturing a trench-gate silicon semiconductor device (1), the method including forming trenches (20) in a semiconductor body (10) in an active transistor cell area of the device, the trenches (20) each having a trench bottom and trench sidewalls, and providing silicon oxide gate insulation (21A, 21B) in the trenches such that the gate insulation (21B, 33) at the trench bottoms is thicker than the gate insulation (21A, 21) at the trench sidewalls, wherein the method includes, after forming the trenches (20), the steps of:

forming a silicon oxide layer (21) at the trench bottoms and trench sidewalls;

depositing a layer of doped polysilicon (31) adjacent the trench bottoms and trench side walls;

forming silicon nitride spacers (32) on the doped polysilicon (21) adjacent the trench sidewalls leaving the doped polysilicon exposed at the trench bottoms;

thermally oxidising the exposed doped polysilicon to grow said thicker gate insulation (33) at the trench bottoms;

removing the silicon nitride spacers (32); and

providing gate conductive material (34) within the trenches.

2. (original) A method as claimed in claim 1, wherein step (b) deposits the layer of doped polysilicon (31) on the silicon oxide layer (21) formed in step (a), and wherein step (d) grows the thicker gate insulation (33) below the nitride spacers (32).

3. (original) A method as claimed in claim 1, including the further step (g) of forming a silicon nitride layer (41) at the trench bottoms and trench sidewalls on the silicon oxide layer (21) which has been formed in step (a), wherein step (b) deposits the layer of doped polysilicon (31) on the silicon nitride layer (41) formed in step (g) such that the silicon nitride layer (41) at the trench bottoms limits the downward growth of the thicker gate insulation (33) in step (d), and wherein the silicon nitride layer (41) is removed from the trench sidewalls before depositing gate conductive material (34) in step (f).

4. (currently amended) A method as claimed in ~~any one of claims 1 to 3~~claim 1, wherein the silicon oxide layer (21) formed at the trench sidewalls in step (a) is retained as trench sidewall gate insulation (21A) before depositing gate conductive material (34) in step (f).

5. (currently amended) A method as claimed in ~~any one of claims 1 to 4~~claim 1, wherein the doped polysilicon (31) deposited in step (b) is greater than 5e19cm-3 As or P doped polysilicon.

6. (currently amended) A method as claimed in ~~any one of claims 1 to 5~~claim 1, wherein in step (d) the doped polysilicon (31) is thermally oxidised at a temperature in the range 650-850°C.

7. (original) A method as claimed in claim 6, wherein the oxidation temperature range is 700-800°C.

8. (currently amended) A trench-gate silicon semiconductor device (1) manufactured by the method as claimed in ~~any one of claims 1 to 7~~claim 1.

9. (original) A device as claimed in claim 8, wherein the device is a vertical power transistor.

10. (original) A device as claimed in claim 9, wherein the transistor cells have a cell pitch less than 2 micron.

11. (currently amended) A device as claimed in claim 9 ~~or claim 10~~, wherein the device (1) has a plurality of electrically parallel

closed transistor cells (TC2) configured in a two-dimensionally repetitive pattern in the active area of the device, wherein a trench network includes segment trench regions (G2S) adjacent sides of the transistor cells (TC2), and wherein said trenches (20) in which the gate insulation is thicker (21B, 33) at said trench bottoms than the gate insulation at said trench sidewalls (21A, 21) comprise the segment trench regions (G2S).

12. (original) A method of manufacturing a trench-gate silicon semiconductor device substantially as herein described with reference to and as shown in Figures 1, 2, 3, and 4A to 4D of the accompanying drawings.

13. (original) A method of manufacturing a trench-gate silicon semiconductor device substantially as herein described with reference to and as shown in Figures 1, 2, 3, and 4A to 4D, as modified by Figures 5A to 5D, of the accompanying drawings.